JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

Results for M.Tech (R13/R09) II Semester Regular/Supply Examinations July-2016

College: ANDHRA LOYOLA INSTT OF ENGG AND TECHNOLOGY, VIJAYAWADA:HP

Discrepancy pertaining to these results are to be submitted on or before 30-01-2017 with following documents at CE(PG) Office,JNTUK,Kakinada

- Online Registration Proof
- Hallticket
- DForm(Online)
- DForm(Offline)
- Attendance Sheet
- Any Other supporting Documents

Htno	Subcode	Subname	Internal	External	credits
12HP1D5802	D5809	DATA WARE HOUSING AND DATA MINING	20	22	0
13HP1D3804	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	11	10	0
13HP1D3807	H3801	CODING THEORY & APPLICATIONS	18	25	0
13HP1D5818	H0501	DATA WAREHOUSING AND DATA MINING	12	20	0
14HP1D5803	H0501	DATA WAREHOUSING AND DATA MINING	12	26	0
14HP1D5805	H2508	CLOUD COMPUTING	20	31	1
14HP1D5805	H4002	INFORMATION SECURITY	16	11	0
14HP1D5805	H5801	COMPUTER NETWORKS	26	10	0
14HP1D5805	H5802	MOBILE COMPUTING ELECTIVE-I	28	24	1
14HP1D5810	H5802	MOBILE COMPUTING ELECTIVE-I	31	35	1
14HP1D5811	H2508	CLOUD COMPUTING	16	25	0
15HP1D3801	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	31	27	3
15HP1D3801	H3801	CODING THEORY & APPLICATIONS	38	49	3
15HP1D3801	H3803	ADVANCED COMMUNICATIONS LAB	38	50	2
15HP1D3801	H4502	IMAGE & VIDEO PROCESSING	34	27	3
15HP1D3801	H4503	WIRELESS COMMUNICATION & NETWORKS	37	31	3
15HP1D3801	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	40	46	3
15HP1D3801	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	35	24	3
15HP1D3802	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	29	37	3
15HP1D3802	H3801	CODING THEORY & APPLICATIONS	38	37	3
15HP1D3802	H3803	ADVANCED COMMUNICATIONS LAB	37	53	2
15HP1D3802	H4502	IMAGE & VIDEO PROCESSING	32	40	3
15HP1D3802	H4503	WIRELESS COMMUNICATION & NETWORKS	39	37	3
15HP1D3802	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	40	38	3
15HP1D3802	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	36	33	3
15HP1D3803	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	29	34	3
15HP1D3803	H3801	CODING THEORY & APPLICATIONS	37	35	3
15HP1D3803	H3803	ADVANCED COMMUNICATIONS LAB	32	47	2
15HP1D3803	H4502	IMAGE & VIDEO PROCESSING	32	29	3
15HP1D3803	H4503	WIRELESS COMMUNICATION & NETWORKS	37	28	3
15HP1D3803	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	37	42	3
15HP1D3803	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	27	30	3
15HP1D3804	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	31	34	3
15HP1D3804	H3801	CODING THEORY & APPLICATIONS	38	51	3

Htno	Subcode	Subname	Internal	External	credits
15HP1D3804	H3803	ADVANCED COMMUNICATIONS LAB	37	48	2
15HP1D3804	H4502	IMAGE & VIDEO PROCESSING	32	32	3
15HP1D3804	H4503	WIRELESS COMMUNICATION & NETWORKS	37	25	3
15HP1D3804	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	38	49	3
15HP1D3804	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	32	28	3
15HP1D3805	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	23	31	3
15HP1D3805	H3801	CODING THEORY & APPLICATIONS	38	43	3
15HP1D3805	H3803	ADVANCED COMMUNICATIONS LAB	35	49	2
15HP1D3805	H4502	IMAGE & VIDEO PROCESSING	26	28	3
15HP1D3805	H4503	WIRELESS COMMUNICATION & NETWORKS	35	28	3
15HP1D3805	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	26	43	3
15HP1D3805	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	23	15	0
15HP1D3806	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	30	26	3
15HP1D3806	H3801	CODING THEORY & APPLICATIONS	35	27	3
15HP1D3806	H3803	ADVANCED COMMUNICATIONS LAB	36	47	2
15HP1D3806	H4502	IMAGE & VIDEO PROCESSING	23	27	3
15HP1D3806	H4503	WIRELESS COMMUNICATION & NETWORKS	31	24	3
15HP1D3806	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	32	39	3
15HP1D3806	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	18	3	0
15HP1D3807	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	31	37	3
15HP1D3807	H3801	CODING THEORY & APPLICATIONS	35	49	3
15HP1D3807	H3803	ADVANCED COMMUNICATIONS LAB	33	47	2
15HP1D3807	H4502	IMAGE & VIDEO PROCESSING	29	39	3
15HP1D3807	H4503	WIRELESS COMMUNICATION & NETWORKS	36	29	3
15HP1D3807	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	40	55	3
15HP1D3807	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	29	34	3
15HP1D3808	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	24	30	3
15HP1D3808	H3801	CODING THEORY & APPLICATIONS	34	26	3
15HP1D3808	H3803	ADVANCED COMMUNICATIONS LAB	31	49	2
15HP1D3808	H4502	IMAGE & VIDEO PROCESSING	32	29	3
15HP1D3808	H4503	WIRELESS COMMUNICATION & NETWORKS	36	24	3
15HP1D3808	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	32	34	3
15HP1D3808	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	22	28	3
15HP1D3809	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	28	27	3
15HP1D3809	H3801	CODING THEORY & APPLICATIONS	35	33	3
15HP1D3809	H3803	ADVANCED COMMUNICATIONS LAB	35	45	2
15HP1D3809	H4502	IMAGE & VIDEO PROCESSING	33	24	3
15HP1D3809	H4503	WIRELESS COMMUNICATION & NETWORKS	35	28	3
15HP1D3809	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	37	38	3
15HP1D3809	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	12	38	3
15HP1D3810	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	24	32	3
15HP1D3810	H3801	CODING THEORY & APPLICATIONS	36	40	3
15HP1D3810	H3803	ADVANCED COMMUNICATIONS LAB	33	55	2
15HP1D3810	H4502	IMAGE & VIDEO PROCESSING	25	40	3
15HP1D3810	H4503	WIRELESS COMMUNICATION & NETWORKS	36	28	3
15HP1D3810	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	29	52	3
15HP1D3810	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	21	34	3
15HP1D3811	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	26	32	3
15HP1D3811	H3801	CODING THEORY & APPLICATIONS	37	32	3
15HP1D3811	H3803	ADVANCED COMMUNICATIONS LAB	32	49	2
15HP1D3811	H4502	IMAGE & VIDEO PROCESSING	32	40	3

Htno	Subcode	Subname	Internal	External	credits
15HP1D3811	H4503	WIRELESS COMMUNICATION & NETWORKS	36	25	3
15HP1D3811	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	28	49	3
15HP1D3811	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	27	36	3
15HP1D3812	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	22	30	3
15HP1D3812	H3801	CODING THEORY & APPLICATIONS	34	35	3
15HP1D3812	H3803	ADVANCED COMMUNICATIONS LAB	36	53	2
15HP1D3812	H4502	IMAGE & VIDEO PROCESSING	26	38	3
15HP1D3812	H4503	WIRELESS COMMUNICATION & NETWORKS	35	30	3
15HP1D3812	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	24	47	3
15HP1D3812	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	26	31	3
15HP1D3813	H0602	CMOS ANALOG AND DIGITAL IC DESIGN	22	34	3
15HP1D3813	H3801	CODING THEORY & APPLICATIONS	34	34	3
15HP1D3813	H3803	ADVANCED COMMUNICATIONS LAB	32	49	2
15HP1D3813	H4502	IMAGE & VIDEO PROCESSING	25	33	3
15HP1D3813	H4503	WIRELESS COMMUNICATION & NETWORKS	30	24	3
15HP1D3813	H6803	EMBEDDED REAL TIME OPERATING SYSTEMS	29	44	3
15HP1D3813	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	23	39	3
15HP1D5801	H0501	DATA WAREHOUSING AND DATA MINING	24	28	3
15HP1D5801	H2508	CLOUD COMPUTING	28	42	3
15HP1D5801	H4002	INFORMATION SECURITY	31	27	3
15HP1D5801	H5801	COMPUTER NETWORKS	24	38	3
15HP1D5801	H5803	COMPILER DESIGN ELECTIVE-I	23	46	3
15HP1D5801	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	34	26	3
15HP1D5801	H5806	CSE LAB-2	35	54	3
15HP1D5802	H0501	DATA WAREHOUSING AND DATA MINING	24	26	3
15HP1D5802	H2508	CLOUD COMPUTING	30	27	3
15HP1D5802	H4002	INFORMATION SECURITY	28	24	3
15HP1D5802	H5801	COMPUTER NETWORKS	26	26	3
15HP1D5802	H5803	COMPILER DESIGN ELECTIVE-I	26	29	3
15HP1D5802	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	34	24	3
15HP1D5802	H5806	CSE LAB-2	32	53	3
15HP1D5803	H0501	DATA WAREHOUSING AND DATA MINING	26	34	3
15HP1D5803	H2508	CLOUD COMPUTING	31	30	3
15HP1D5803	H4002	INFORMATION SECURITY	33	27	3
15HP1D5803	H5801	COMPUTER NETWORKS	36	37	3
15HP1D5803	H5803	COMPILER DESIGN ELECTIVE-I	27	42	3
15HP1D5803	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	34	28	3
15HP1D5803	H5806	CSE LAB-2	37	52	3
15HP1D5804	H0501	DATA WAREHOUSING AND DATA MINING	23	36	3
15HP1D5804	H2508	CLOUD COMPUTING	29	33	3
15HP1D5804	H4002	INFORMATION SECURITY	29	24	3
15HP1D5804	H5801	COMPUTER NETWORKS	24	39	3
15HP1D5804	H5803	COMPILER DESIGN ELECTIVE-I	24	35	3
15HP1D5804	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	33	34	3
15HP1D5804	H5806	CSE LAB-2	36	52	3
15HP1D5805	H0501	DATA WAREHOUSING AND DATA MINING	27	24	3
15HP1D5805	H2508	CLOUD COMPUTING	23	27	3
15HP1D5805	H4002	INFORMATION SECURITY	23	15	0
15HP1D5805	H5801	COMPUTER NETWORKS	22	32	3
15HP1D5805	H5803	COMPILER DESIGN ELECTIVE-I	22	35	3
15HP1D5805	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	24	15	0

Htno	Subcode	Subname	Internal	External	credits
15HP1D5805	H5806	CSE LAB-2	33	50	3
15HP1D5806	H0501	DATA WAREHOUSING AND DATA MINING	32	26	3
15HP1D5806	H2508	CLOUD COMPUTING	37	36	3
15HP1D5806	H4002	INFORMATION SECURITY	34	27	3
15HP1D5806	H5801	COMPUTER NETWORKS	29	42	3
15HP1D5806	H5803	COMPILER DESIGN ELECTIVE-I	28	28	3
15HP1D5806	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	32	30	3
15HP1D5806	H5806	CSE LAB-2	37	60	3
15HP1D5807	H0501	DATA WAREHOUSING AND DATA MINING	22	28	3
15HP1D5807	H2508	CLOUD COMPUTING	23	31	3
15HP1D5807	H4002	INFORMATION SECURITY	27	12	0
15HP1D5807	H5801	COMPUTER NETWORKS	24	26	3
15HP1D5807	H5803	COMPILER DESIGN ELECTIVE-I	20	30	3
15HP1D5807	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	28	27	3
15HP1D5807	H5806	CSE LAB-2	35	52	3
15HP1D5808	H0501	DATA WAREHOUSING AND DATA MINING	28	34	3
15HP1D5808	H2508	CLOUD COMPUTING	35	26	3
15HP1D5808	H4002	INFORMATION SECURITY	37	28	3
15HP1D5808	H5801	COMPUTER NETWORKS	29	29	3
15HP1D5808	H5803	COMPILER DESIGN ELECTIVE-I	28	46	3
15HP1D5808	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	39	48	3
15HP1D5808	H5806	CSE LAB-2	39	56	3
15HP1D5809	H0501	DATA WAREHOUSING AND DATA MINING	20	30	3
15HP1D5809	H2508	CLOUD COMPUTING	21	29	3
15HP1D5809	H4002	INFORMATION SECURITY	30	28	3
15HP1D5809	H5801	COMPUTER NETWORKS	31	36	3
15HP1D5809	H5803	COMPILER DESIGN ELECTIVE-I	30	28	3
15HP1D5809	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	30	36	3
15HP1D5809	H5806	CSE LAB-2	34	59	3
15HP1D5810	H0501	DATA WAREHOUSING AND DATA MINING	29	39	3
15HP1D5810	H2508	CLOUD COMPUTING	33	37	3
15HP1D5810	H4002	INFORMATION SECURITY	36	42	3
15HP1D5810	H5801	COMPUTER NETWORKS	34	36	3
15HP1D5810	H5803	COMPILER DESIGN ELECTIVE-I	32	42	3
15HP1D5810	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	38	33	3
15HP1D5810	H5806	CSE LAB-2	40	57	3

**Note:1)For Recounting/Revaluation/Challenge By Revaluation Apply through Online(www.jntukresults.edu.in))

NOTE:2 [Last Date for Apply Recounting/Revaluation/Challenge By Revaluation: **03-02-2017]

**NOTE:3 [Please inform to the students to enter these subject codes for applying Recounting/Revaluation/Challenge By Revaluation]

**NOTE:4
[-1 in the filed of externals indicates student absent for the respective subject.

-2 in the filed of externals indicates student result is withheld for the respective subject.

-3 in the filed of externals indicates Malpractice for the respective subject.]

Date:21-01-2017

Controller of Examinations

PRINCIPAL
ANDHRA LOYOLA INSTITUTE OF
ENGINEERING & TECHNOLOGY
VIJAYAWADA-520008.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

Results for M.Tech II SEMESTER(R13/R16) Regular/Supplementary Examinations, MAY-2017.

College: ANDHRA LOYOLA INSTT OF ENGG AND TECHNOLOGY, VIJAYAWADA:HP

Discrepancy pertaining to these results are to be submitted on or before 20-12-2017 with following documents at CE(PG) Office,JNTUK,Kakinada

Htno	Subcode	Subname	Internal	External	credits
13HP1D3807	H3801	CODING THEORY & APPLICATIONS	18	28	0
15HP1D3805	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	23	19	0
15HP1D3806	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	18	16	0
15HP1D5805	H4002	INFORMATION SECURITY	23	26	0
15HP1D5805	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	24	24	0
15HP1D5807	H4002	INFORMATION SECURITY	27	34	1
16HP1D3801	J0601	CMOS ANALOG AND DIGITAL IC DESIGN ELECTI	36	24	1
16HP1D3801	J3801	CODING THEORY AND APPLICATIONS	35	41	1
16HP1D3801	J3804	ADVANCED COMMUNICATIONS LABORATORY	39	57	1
16HP1D3801	J4502	IMAGE AND VIDEO PROCESSING	38	31	1
16HP1D3801	J4508	WIRELESS COMMUNICATIONS AND NETWORKS ELE	37	30	1
16HP1D3801	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	38	26	1
16HP1D3801	J6805	DSP PROCESSORS AND ARCHITECTURES	37	46	1
16HP1D3802	J0601	CMOS ANALOG AND DIGITAL IC DESIGN ELECTI	38	28	1
16HP1D3802	J3801	CODING THEORY AND APPLICATIONS	38	50	1
16HP1D3802	J3804	ADVANCED COMMUNICATIONS LABORATORY	38	58	1
16HP1D3802	J4502	IMAGE AND VIDEO PROCESSING	39	42	1
16HP1D3802	J4508	WIRELESS COMMUNICATIONS AND NETWORKS ELE	37	40	1
16HP1D3802	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	38	33	1
16HP1D3802	J6805	DSP PROCESSORS AND ARCHITECTURES	36	57	1
16HP1D3803	J0601	CMOS ANALOG AND DIGITAL IC DESIGN ELECTI	37	27	1
16HP1D3803	J3801	CODING THEORY AND APPLICATIONS	38	43	1
16HP1D3803	J3804	ADVANCED COMMUNICATIONS LABORATORY	37	55	1
16HP1D3803	J4502	IMAGE AND VIDEO PROCESSING	39	34	1
16HP1D3803	J4508	WIRELESS COMMUNICATIONS AND NETWORKS ELE	37	32	1
16HP1D3803	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	38	37	1
16HP1D3803	J6805	DSP PROCESSORS AND ARCHITECTURES	32	56	1
16HP1D3804	J0601	CMOS ANALOG AND DIGITAL IC DESIGN ELECTI	32	27	1
16HP1D3804	J3801	CODING THEORY AND APPLICATIONS	38	46	1
16HP1D3804	J3804	ADVANCED COMMUNICATIONS LABORATORY	39	56	1
16HP1D3804	J4502	IMAGE AND VIDEO PROCESSING	38	38	1
16HP1D3804	J4508	WIRELESS COMMUNICATIONS AND NETWORKS ELE	37	36	1
16HP1D3804	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	39	38	1
16HP1D3804	J6805	DSP PROCESSORS AND ARCHITECTURES	33	60	1
16HP1D3805	J0601	CMOS ANALOG AND DIGITAL IC DESIGN ELECTI	32	25	1
16HP1D3805	J3801	CODING THEORY AND APPLICATIONS	30	35	1
16HP1D3805	J3804	ADVANCED COMMUNICATIONS LABORATORY	36	50	1
16HP1D3805	J4502	IMAGE AND VIDEO PROCESSING	32	32	1
16HP1D3805	J4508	WIRELESS COMMUNICATIONS AND NETWORKS ELE	33	25	1
16HP1D3805	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	31	32	1
16HP1D3805	J6805	DSP PROCESSORS AND ARCHITECTURES	26	47	1

Htno	Subcode	Subname	Internal	External	credits
16HP1D3806	J0601	CMOS ANALOG AND DIGITAL IC DESIGN ELECTI	25	25	1
16HP1D3806	J3801	CODING THEORY AND APPLICATIONS	34	25	1
16HP1D3806	J3804	ADVANCED COMMUNICATIONS LABORATORY	35	51	1
16HP1D3806	J4502	IMAGE AND VIDEO PROCESSING	36	39	1
16HP1D3806	J4508	WIRELESS COMMUNICATIONS AND NETWORKS ELE	31	28	1
16HP1D3806	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	35	28	1
16HP1D3806	J6805	DSP PROCESSORS AND ARCHITECTURES	27	50	1
16HP1D3807	J0601	CMOS ANALOG AND DIGITAL IC DESIGN ELECTI	33	24	1
16HP1D3807	J3801	CODING THEORY AND APPLICATIONS	35	41	1
16HP1D3807	J3804	ADVANCED COMMUNICATIONS LABORATORY	37	56	1
16HP1D3807	J4502	IMAGE AND VIDEO PROCESSING	37	44	1
16HP1D3807	J4508	WIRELESS COMMUNICATIONS AND NETWORKS ELE	31	39	1
16HP1D3807	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	38	36	1
16HP1D3807	J6805	DSP PROCESSORS AND ARCHITECTURES	28	56	1
16HP1D3808	J0601	CMOS ANALOG AND DIGITAL IC DESIGN ELECTI	31	26	1
16HP1D3808	J3801	CODING THEORY AND APPLICATIONS	35	37	1
16HP1D3808	J3804	ADVANCED COMMUNICATIONS LABORATORY	36	58	1
16HP1D3808	J4502	IMAGE AND VIDEO PROCESSING	35	33	1
16HP1D3808	J4508	WIRELESS COMMUNICATIONS AND NETWORKS ELE	35	29	1
16HP1D3808	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	35	24	1
16HP1D3808	J6805	DSP PROCESSORS AND ARCHITECTURES	28	53	1
16HP1D3809	J0601	CMOS ANALOG AND DIGITAL IC DESIGN ELECTI	30	29	1
16HP1D3809	J3801	CODING THEORY AND APPLICATIONS	34	34	1
16HP1D3809	J3804	ADVANCED COMMUNICATIONS LABORATORY	35	50	1
16HP1D3809	J4502	IMAGE AND VIDEO PROCESSING	35	32	1
16HP1D3809	J4508	WIRELESS COMMUNICATIONS AND NETWORKS ELE	32	34	1
16HP1D3809	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	32	15	0
16HP1D3809	J6805	DSP PROCESSORS AND ARCHITECTURES	27	57	1
16HP1D5802	J0502	SOFTWARE ENGINEERING ELECTIVE I	39	37	1
16HP1D5802	J2503	CYBER SECURITY	39	31	1
16HP1D5802	J4001	ADVANCED UNIX PROGRAMMING	39	24	1
16HP1D5802	J4002	BIG DATA ANALYTICS	36	41	1
16HP1D5802	J5801	COMPUTER NETWORKS	39	26	1
16HP1D5802	J5802	MOBILE COMPUTING ELECTIVE II	37	42	1
16HP1D5802	J5803	CSE LAB 2	37	58	1
16HP1D5803	J0502	SOFTWARE ENGINEERING ELECTIVE I	39	44	1
16HP1D5803	J2503	CYBER SECURITY	39	48	1
16HP1D5803	J4001	ADVANCED UNIX PROGRAMMING	38	35	1
16HP1D5803	J4002	BIG DATA ANALYTICS	38	45	1
16HP1D5803	J5801	COMPUTER NETWORKS	38	44	1
16HP1D5803	J5802	MOBILE COMPUTING ELECTIVE II	37	50	1
16HP1D5803	J5803	CSE LAB 2	38	58	1

**Note:1)For Recounting/Revaluation/Challenge By Revaluation Apply through Online(www.jntukresults.edu.in))

NOTE:2 [Last Date for Apply Recounting/Revaluation/Challenge By Revaluation: **27-12-2017]

**NOTE:3 [Please inform to the students to enter these subject codes for applying Recounting/Revaluation/Challenge By Revaluation]

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-2 in the filed of externals indicates student result is withheld for the respective subject.

-3 in the filed of externals indicates Malpractice for the respective subject.]

Date:06-12-2017

Controller of Examinations

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ENGINEERING & TECHNOLO
VIJAYAWADA-520008.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

Results for M.Tech II SEMESTER (R16 / R13) Regular / Supplementary Examinations , JUNE- 2018 .

College: ANDHRA LOYOLA INSTT OF ENGG AND TECHNOLOGY, VIJAYAWADA:HP

Discrepancy pertaining to these results are to be submitted on or before 24-09-2018 with following documents at CE(PG) Office,JNTUK,Kakinada

Htno	Subcode	Subname	Internal	External	credits
14HP1D5811	H2508	CLOUD COMPUTING	16	22	0
15HP1D3805	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	23	36	1
15HP1D3806	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	18	17	0
15HP1D5805	H4002	INFORMATION SECURITY	23	27	1
15HP1D5805	H5804	OBJECT ORIENTED ANALYSIS AND DESIGN ELEC	24	28	1
16HP1D3809	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	32	30	1
17HP1D3801	J0601	CMOS ANALOG AND DIGITAL IC DESIGN ELECTI	36	33	1
17HP1D3801	J3801	CODING THEORY AND APPLICATIONS	37	50	1
17HP1D3801	J3804	ADVANCED COMMUNICATIONS LABORATORY	39	58	1
17HP1D3801	J4502	IMAGE AND VIDEO PROCESSING	38	56	1
17HP1D3801	J4508	WIRELESS COMMUNICATIONS AND NETWORKS ELE	39	38	1
17HP1D3801	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	38	32	1
17HP1D3801	J6805	DSP PROCESSORS AND ARCHITECTURES	38	46	1
17HP1D3802	J0601	CMOS ANALOG AND DIGITAL IC DESIGN ELECTI	37	24	1
17HP1D3802	J3801	CODING THEORY AND APPLICATIONS	36	27	1
17HP1D3802	J3804	ADVANCED COMMUNICATIONS LABORATORY	34	45	1
17HP1D3802	J4502	IMAGE AND VIDEO PROCESSING	34	29	1
17HP1D3802	J4508	WIRELESS COMMUNICATIONS AND NETWORKS ELE	33	24	1
17HP1D3802	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	37	29	1
17HP1D3802	J6805	DSP PROCESSORS AND ARCHITECTURES	33	24	1
17HP1D3803	J0601	CMOS ANALOG AND DIGITAL IC DESIGN ELECTI	36	24	1
17HP1D3803	J3801	CODING THEORY AND APPLICATIONS	35	33	1
17HP1D3803	J3804	ADVANCED COMMUNICATIONS LABORATORY	37	54	1
17HP1D3803	J4502	IMAGE AND VIDEO PROCESSING	34	37	1
17HP1D3803	J4508	WIRELESS COMMUNICATIONS AND NETWORKS ELE	34	24	1
17HP1D3803	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	37	32	1
17HP1D3803	J6805	DSP PROCESSORS AND ARCHITECTURES	34	28	1
17HP1D3804	J0601	CMOS ANALOG AND DIGITAL IC DESIGN ELECTI	36	34	1
17HP1D3804	J3801	CODING THEORY AND APPLICATIONS	36	37	1
17HP1D3804	J3804	ADVANCED COMMUNICATIONS LABORATORY	38	56	1
17HP1D3804	J4502	IMAGE AND VIDEO PROCESSING	36	39	1
17HP1D3804	J4508	WIRELESS COMMUNICATIONS AND NETWORKS ELE	35	26	1
17HP1D3804	J6801	EMBEDDED SYSTEM DESIGN ELECTIVEIII	38	38	1
17HP1D3804	J6805	DSP PROCESSORS AND ARCHITECTURES	33	39	1

**Note:1)For Recounting/Revaluation/Challenge By Revaluation Apply through Online(www.jntukresults.edu.in))

NOTE:2 [Last Date for Apply Recounting/Revaluation/Challenge By Revaluation: **01-10-2018]

NOTE:2 [Last Date for Apply Recounting/Revaluation/Challenge By Revaluation: **16-11-2019]

**NOTE:3 [Please inform to the students to enter these subject codes for applying Recounting/Revaluation/Challenge By Revaluation]

**NOTE:
[-1 in the filed of externals indicates student absent for the respective subject.

-2 in the filed of externals indicates student result is withheld for the respective subject.

-3 in the filed of externals indicates Malpractice for the respective subject.]

N. Mohan Rao

Date:02-11-2019

Controller of Examinations

PRINCIPAL
ANDHRA LOYOLA INSTITUTE OF
ENGINEERING & TECHNOLOGY
VIJAYAWADA-520008.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

Results of M.TECH II SEMESTER (R16) EXAMINATIONS, OCTOBER-2021

College name: ANDHRA LOYOLA INSTT OF ENGG AND TECHNOLOGY, VIJAYAWADA(HP

Htno	Subcode	Subname	Internal	External	CREDITS
18HP1D3801	J4502	IMAGE AND VIDEO PROCESSING	38	47	1

**Note:1)[Last Date to apply for Recounting/Revaluation/Challenge Revaluation is : 04-02-2022]

** Note:**

* -1 in the filed of externals indicates student is absent for the respective subject.

* -2 in the filed of externals indicates student result Withheld for the respective subject.

* -3 in the filed of externals indicates student involved in Malpractice for the respective subject.

Controller of Examinations

Date:27.01.2022

PRINCIPAL
ANDHRA LOYOLA INSTITUTE OF
ENGINEERING & TECHNOLOGY
VIJAYAWADA-52

Grams: "TECHNOLOGY"
Email : cepgprojects.jntuk@gmail.com

Off: 0884-2300907
0884-2300902

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA
Kakinada-533003, Andhra Pradesh, India

Lr. No: CE/JNTUK/Project-Viva-Voce/D8/HP/2021 Date : 17.04.2021

Dr. K VENKATA REDDY
B.Tech., M.Tech., Ph.D
Controller of Examinations.

To
The Principal,
Andhra Loyola Institute of Engineering & Technology
Vijayawada – 520 008,
Krishna Dist.

Sub: – M. Tech Project Thesis Evaluation – Appointment of External Examiner-Intimation-Reg.
Ref: – Letter from Andhra Loyola Institute of Engg. & Technology, Vijayawada,,. Dated : 05.03.2021.

In response to the letter cited above, as per the directions, the details of the external examiner for conduct of Project Viva-Voce Examination of M. Tech Students are as given below:

S. No	Hall Ticket No.	Details of the Examiner	Contact Details
1	18HP1D3802	Dr. G Chenchemma Professor in ECE, VIT For Women College, Krishna dt	M : 7569186949 Email : chenchemma.limat@gmail.com
2	18HP1D3803		
3	18HP1D3804		
4	18HP1D3805		

The external examiner is requested to evaluate the soft copy of the thesis and submit the corrections, if any, to the Principal of the concerned college through email in the format enclosed. The Principals are requested to communicate the corrections suggested by the external examiner to HOD and the project Guide. The Candidates are required to incorporate the corrections/ Modifications suggested by the external examiner is the final thesis before the conduct of Viva-Voce.

It is informed that the examiners have to be contacted and conduct viva – voce examination is to be conducted Online through Video conferencing as per the guidelines issued by the University Examination branch within two weeks from the date of appointment order as per M. Tech/~~M.Pharmacy/MCA/MBA~~ Regulations of the University. The college has to pay to the examiner @ Rs.750/- for evaluation of thesis and Rs.750/- for conducting Viva-Voce examination per candidate in addition to eligible TA and DA.

It is further informed that the adjudication/Viva-Voce Examination reports have to be dispatched to the Controller of Examinations, JNTUK Kakinada soon after the completion of Viva-Voce examination along with a soft copy in pdf format of the final thesis.

Sd/-
Controller of Examinations

Copy to the External Examiner.

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VIJAYAWADA-52