ANDHRA LOYOLA INSTITUTE OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ECE

A One Week COURSE ON Digital Design through Verilog HDL

PROGRAM SCHEDULE

S.NO	DAY	SESSION	TOPICS TO BE COVERED
1	22-04-2019	9:00 TO 10:45	Basics of Digital Design Logic Gates, Multiplexers, Decoders, comparators, Flip-flops, Registers and counters.
		11:00 TO 1:00	Basics of Verilog, Levels of Design Description.
2	23-04-2019	9:00 TO 10:45	Language Constructs and Conventions in Verilog Keywords, Identifiers, Datatypes, Operators.
		11:00 TO 1:00	Xilinx Tool DesignFlow, Practice session-1
3	24-04-2019	9:00 TO 10:45	Gate Level Modelling, Practice session-2
		10:45 TO 1:00	Behavioral Modeling, operations and assignments,Intial Consructs,Always construct Examples, Practice session-3
4	25-04-2019	9:00 TO 10:45	Blocking and Non Blocking Statements,If then else ,case statement. Practice session-4
		11:00 TO 1:00	For Loop,whileloop,Foreverloop.,Practice session-5
5	25-04-2019	9:00 TO 10:45	Data Flow Modelling
		11:00 TO 1:00	Practice session-6
6	26-04-2019	9:00 TO 10:45	Project1
		11:00 TO 1:00	Project2