Andhra Loyola Institute of Engineering and Technology:: Vijayawada.

FACULTY PROFILE

Name of the Faculty	Ms. K Mariya Priyadarshini		
Designation	Asst.Prof.		
Department	Electronics and Communication Engineering		
Date of joining	01-05-2023		
Qualification With class/Grade	UG: B.Tech, 1st class		
	PG: M.Tech, 1st class with distinction		
Employee ID	ALIET-23-09		
E-mail	mariyapriyadarshini@gmail.com		
Total Experience in Years	Teaching: 8 Years	Industry: 00 Years	Research: 00 Years
Papers published	National: 0		International: 25
Ph.D Guide? Give field University	Field:--		University:--
PhDs /Projects guided	PhDs: 00		Projects at PG Level: 9 9
			Projects at UG Level: 3 20
Books published/IPRs/Patents	---		
Professional Memberships			
Consultancy Activities	--		
Awards	--		
Grants fetched	--		
Whether Ratified by University (Yes/No)	**Yes**		

OTHER ACHIEVEMENTS

Did certified courses on

1. VLSI CAD Part II: Layout
2. Getting Started with AI using IBM Watson
3. Introduction to Artificial Intelligence (AI)
4. AI Foundations for Everyone
5. Building AI Powered Chatbots Without Programming
6. Programming for Everybody (Getting Started with Python)

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WORK EXPERIENCE: 8 Years

College **:**SRK Institute of Technology, Vijayawada

Position **:** Assistant Professor, Dept. of Electronics and Communication Engineering

Experience **:** 5 years i.e. (1-06-2011 to 30-04-2016)

College **:** KLEF Deemed to be University, Guntur

Position **:** Assistant Professor, Dept. of Electronics and Communication Engineering

Experience **:** 2 years 11Months i.e. (13-07-2017 to 14-06-2022)

Details of Research Program: Thesis submitted, Registered for Ph.D at KLEF Deemed to be University, Guntur on Jan-2018.

PUBLICATIONS: International Journals

1. Flavia Princess Nesamani, I, J.Kanaka deva Princy , K.MariaPriyadharshini Dr.V.LakshmiPrabha, “An Architectural Framework for Power Performance Tuning”, CIIT International Journal of Programmable Device Circuits and Systems, Vol.3 & No.2, February 2011, pp.86-90.
2. Flavia Princess Nesamani, I, K.MariaPriyadharshini, J.Kanaka deva Princy Dr.V.LakshmiPrabha, “A Novel Optimization Technique for Multi Domain Clock Skew Scheduling”, CIIT International Journal of Programmable Device Circuits and Systems, Vol.3 & No.2, February 2011,pp.81-85.
3. K. Mariya Priyadarshini , K.Gnana Deepika,K.David Solomon Raju , “sleepy keeper approach for power performance tuning in VLSI design”, International Journal of Electronics and

Communication Engineering (IJECE- 2013) ISSN 0974-2166 Volume 6, Number 1 (2013), pp. 17-28

4. K Mariya Priyadarshini, Ch,Sreedhar, “Low Power and Reduce Area Dual Edge Pulse Triggered Flip-Flop Based on Signal Feed-Through Scheme”International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE), Volume 3, Issue11, November 2014.

5. K. Mariya Priyadarshini, N.V.N Ravikiran, N. Tejasri, T.C Venkat Anish, “Design Of Area And Speed Efficient Square Root Carry Select Adder Using Fast Adders”International journal of scientific and Technical Research(IJSTR), volume 3,Issue 6, June 2014.

6. K.Mariya Priyadarshini , V.Kailash, , M.Abhinaya, K.Prashanthi, Y.Kannaji, “Low Power State Retention Technique for Low Power VLSI design” International Journal of Advanced Computer Research (IJACR), (ISSN (print): 2249-7277 ISSN (online): 2277-7970), Volume-4 Number-2 Issue-15 June-2014.

7. K. Mariya Priyadarshini, M. Naga Sabari, “Comparative Analysis of a Low Power and High Speed Hybrid 1-Bit Full Adder for ULSI Circuits” International Journal of Science and Research (IJSR), ISSN (Online): 2319-7064, Volume 5 Issue 9, September 2016.

8. K Mariya Priyadarshini, Dr.R.S.Ernest Ravindran, “Novel Two Fold Edge Activated Memory Cell with Low Power Dissipation and High Speed”, International Journal of Recent Technology and EngineeringVolume 8, Issue 1, May 2019, Pages 1491-1495.

9. K Mariya Priyadarshini, Dr.R.S.Ernest Ravindran, P. Ratna Bhaskar, “A Detailed Scrutiny and Reasoning on VLSI Binary
Adder Circuits and Architectures”International Journal of Innovative Technology and Exploring EngineeringVolume 8, Issue 7, May 2019, Pages 887-895

10. R. S. Ernest Ravindran, K Mariya Priyadarshini, Dangeti Peda Manikya Pavana Teja, Popuri Nikhil Chakravarthy, Peruboyina Dharma Teja, “Design of RAM using Quantum Cellular Automata (QCA) Designer”, International Journal of Scientific and Technology Research, Volume 8, Issue 8, August 2019 ISSN 2277-8616, Pages 1385-1390.

11. D Naveen Sai , Surya Kranth G, Paradhasaradhi D, R.S Ernest Ravindran, Lakshmana Kumar M, K Mariya Priyadarshini, Five Input Multilayer Full Adder by QCA Designer” 3rd International Conference on Advances in Computing and Data Sciences, ICACDS 2019; Ghazibad India, 12 April 2019 through 13 April 2019”

12. R.S. Ernest Ravindran, Mariya Priyadarshini, Kavuri Mahesh, Vanga Krishna Vamsi , Chaitanya Eswar , Bishan Yasaswi,” A Novel 24T Conventional adder vs Low Power Reconstructable Transistor Level Conventional Adder”, International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249-8958, Volume-8 Issue-5, June 2019, Pages 398-402.

13. K.Mariya Priyadarshini, Sampad Kumar Panda, R.S. Ernest Ravindran, S Sarvani, P Mohan Vinay, B Suresh Gopi Chand”Performance Analysis of Dual Edge Triggered Memory Cells using Multiple C-Elements” International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-8 Issue-4, November 2019.

14. K.Mariya Priyadarshini , Vipul Agarwal , R.S. Ernest Ravindran , T.Hareesh , B.Harsha , G.V. Kalayan “Design of Low-Power, Area Efficient 2-4 and 4-16 Mixed-Logic Line Decoders” Jour of Adv Research in Dynamical & Control Systems, Vol. 11, Special Issue-08, 2019.

15. K.Mariya Priyadarshini, T.P.S. Kumar Kusumanchi, R.S. Ernest Ravindran, E.Naga Lakshmi bhavani, K.Lahari, P.Maheswari "Low Power High Speed Robust SRAM Cells" International Journal of Advanced Science and Technology Vol. 28, No. 20, (2019), pp. 53-62.

16. R. S Ernest Ravindran , K. Mariya Priyadarshini , A. Thanusha sai , P. Shiny, Sk. Sabeena "Design of Finite field Multiplier for Efficient Data Encryption" International Journal of Advanced Science and Technology Vol. 28, No. 20, (2019), pp. 42-52.

17. K. Mariya Priyadarshini , R. S. Ernest Ravindran , M. Atindra Chandra Sekhar , P. J. V. Sai Kalyan , G. Rahul "A High-Speed Precision-Controllable Approximate 16 bit Multiplier" International Journal of Advanced Science and Technology Vol. 28, No. 20, (2019), pp. 31-41

18. K. Mariya Priyadarshini,Vipul Agarwal, R. S Ernest Ravindran, K. Mercy Romitha, Pritika Kanchan, Kurra Harshita"Logical Fault Modelling Algorithm for Stuck-at-fault", International Journal of Recent Technology and Engineering (IJRTE) ISSN: 2277-3878, Volume-8 Issue-5, January 2020.

19. Priyadarshini, K.M., Ernest Ravindran, R.S., Kumar, R.V., ...Sai Bhattar, S.S., Pavan Sri Kalian, T. "Design and implementation of dual edge triggered shift registers for iot applications", International Journal of Scientific and Technology Research, 2019, 8(10), pp. 3585–3594
20. K Mariya Priyadarshini , R.S Ernest Ravindran , Ipseeta Nanda "A Novel Two Level Edge Activated Carry Save Adder for High Speed Processors" (IJACSA) International Journal of Advance d Computer Science and Applications, Vol. 11, No. 4, May 2020.

21. Priyadarshini, K.M., Ravindran, R.S.E., Sujatha, M., Kumar, K.T.P.S." High-speed pre-accumulator and post-multiplier for convolution neural networks with low power consumption", International Journal of Internet Protocol Technologythis link is disabled, 2022, 15(3-4), pp. 139–147

PUBLICATIONS: International /National Conferences

1. Mariya Priyadarshini, K., Ernest Ravindran, R.S., Krishna, S.V., Durga Bhavani, K. "Design of Compact and Smart Full Adders for High-Speed Nanometer Technology IC's" , Journal of Physics: Conference Seriesthis link is disabled, 2021, 1804(1), 012152.
2. I.Flavia Princess Nesamani, K.Mariya Priyadarshini, Dr.V.Lakshmi Prabha, **"A Novel Approach for Multi- Domain Clock Skew Scheduling" ,** International Conference on VLSI, Communication & Instrumentation (ICVCI) 2011, Proceedings published by International Journal of Computer Applications® (IJCA).
3. **Flavia Princess Nesamani.I,** K.Maria Priyadarshini,et.al, **"Clock Period Optimization Technique Using Multiple Clocking Domains",** Proceeding of IEEE sponsored 3rdInternational Conference on Electronics Computer Technology;(published in IEEE explore), Vol.5-335, April 2011

CONFERENCES/FACULTY DEVELOPMENT PROGRAMS/WORKSHOPS ATTENDED

1. A Two day Workshop on “Issues in Integrated Circuits Design” held during 13th - 14th December 2013, organized by the department of Electronics and Communication Engineering, Gudlavalleru Engineering college, Gudlavalleru, Andhra Pradesh.
2. Participated in two day Faculty Development program on Real Time Signal & Image Processing using XILINX Vivado and Zynq-7000 SOC” organized by department of Electronics and Communication Engineering SRK Institute of technology, Vijayawada during Sept 11-12,2015.
3. Participated in FACULTY DEVELOPMENT PROGRAMME (FDP) ON DNA of Mixed Signal IC design for portable Systems (20th – 25 th May, 2019) Organized at Department of ECE, NIT Warangal.
4. One day training session on “Transactional Analysis” held during 03 January 2019, organized by the department of ECE KLEF deemed to be University
5. One Week FDP on “Low Power MOS Circuit Design and Testing” MEIT, Govt. of INDIA sponsored, organized by E&ICT Academy, National Institute of Technology Warangal at KLEF Vaddeswaram, Andhra Pradesh from 24th-29th june-2019.
6. One day national workshop on “Recent Trends in MEMS devices for IOT Applications” organized by Micro Electronics Research Group(MERG) Department of ECE,KLEF Deemed to be University on 27th December 2019.