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COVID-19 LOCKDOWN IN INDIA: EFFECT ON KEY INDUSTRIES AND UNEMPLOYMENT

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ABSTRACT

This study examine the effect of Covid-19 lockdown on key industries and unemployment. The result prove that based on the length of the lockdown, the Indian economy is likely to face a loss of about 10-31% of its GDP. International Labour Organization report says that more than 40 crore informal workforce in India may get pushed into deeper poverty due to the covid restrictions. This article discuss the effect of Covid-19 lockdown on various industries such as manufacturing,financial services, mining & quuarying, construction, agriculture, forestry&fishing. This paper also demonestrates the impact of Covid-19 lockdown on unemployment. The research is based on secondary in nature wherein plan is to analyze the effect of the Covid-19 lockdown on key sectors and unemployment. The methodology contains reviews, examination of publshed journals, articles and experts discussions. The study revealed that sectoral effect of covid-19 lockdown is continuing and adverse. This study would be useful to the policy makers, Industries, Academic Institutions aswell as student community.

Keywords: Covid-19, Gross Domestic product, Unemployment.

INTRODUCTION

Corona Virus was first identified in Wuhan City of China and by the time the severity of the infectious disease made known to the world; it has spread and started showing its impact globally. India is now part of globalised economy and has great connectivity with rest of the world in terms of import and export of goods and services and people migrating in and out for various purposes. India is one among the 200 plus countries which are hit by the pandemic. Inadequate medical facilities, larger population living in villages and remote locations away from minimum medical aids, less infrastructural facilities; the spread of contagious disease would have been more pathetic than anyone can imagine. In the given circumstances, Government of India was left with no option other than to opt for lockdown compromising on economic health for protecting people. The impact of pandemic and subsequent lockdown decision is very high on industries as well as employment. Various sectors, imports and exports, lives of economically marginalized workers, migrant labour and vulnerable sections of the society have been negatively impacted to note some.

LITERATURE REVIEW

Richard Baldwin., et al. (2020) noted that Covid-19 to be both a supply as well as demand shock which will crash international trade in goods and services and the study concluded that there is a chance of permanent damage to trade system driven by firm's reactions and policy. *Scott R. Baker., et al. (2020)* was observed that Covid-19 strongly impact stock market due to various reasons i.e. it affects public health and economy, inter connection among economies. *ShloloMaital., et al.(2020)* found that the major impact of Covid-19 outbreak would be on supply side of the market, but the remedies being considered currently is mainly focusing on the demand side. The study also pointed that under reasonable current scenarios, a global recession is much likely to occur. *Abiad.,A. et al.(2020)* study estimates that covid-19 would affect global GDP by 0.1 to 0.4% or $77 billion to $347 billion. *Mahendra Dev., S. (2020*) analyzed measures such as lockdown, restrictions on global trade, closure of non-essential services, restriction on movement will adversely affect the financial health of the nation. *Mishra.,*

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Implementation of a Novel 51-Level Asymmetrical Cascaded Multilevel Inverter for Photo-Voltaic Application

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Abstract In general, multilevel inverter plays a key role in present high and medium power operations. This paper proposes a concept of Grid connected PV system with multilevel inverter topology. Mathematical analysis is employed to implement the PV system, and a DC-DC boost converter based on MPPT is used to enhance the PV system's performance. The perturb and observe MPPT approach is used in this paper. For obtaining better harmonic distortions and proper synchronization with grid a multi-level inverter is implemented. This paper proposes a novel multilevel inverter topology for renewable energy operations which produces 31 and 51 level output voltages. The 31-level topology is formed with 10 IGBT switches. A closed loop controller with sinusoidal pulse width modulation technique is implemented to generate gate signals required for 31-Level converter. The 51-Level converter is modelled with 8-IGBT switches and 4-diodes, also space vector and sinusoidal pulse width modulation techniques are used to generate the gate signals for switches. In MATLAB, the proposed system is tested and validated, and a comparison between sinusoidal and space vector modulation in 51-Level topology is conducted.

Keywords photovoltaic (PV), 31 Level and 51 Level Multi-level inverter, total harmonic distortion (THD)

I. Introduction

The day to day increase of population and rapid changes in utilization of electrical power causes deficiency in generation demand. The alternate renewable energy sources helps to meet these requirements. The photovoltaic system plays a key role in distributed energy sources (non-conventional sources) because of freely available in nature and its high reliability. An MPPT based dc-dc converter is implemented to improve the reliability of PV system [2]. The voltage source converter helps to maintain proper synchronization between PV and Grid system. The reference signal for dc-dc converter generated using MPPT controller.

As the output from PV system is in DC nature, so inverter is required to convert it into AC mode. The main disadvantage of basic classical inverter produces high amount of harmonic distortion. The possible solution to get low harmonics is to implement a multi-level inverter. Multilevel inverter have plant their place in medium and high power applications such as Var-Compensators, motor drives and controlling equipments. As the input of inverter is DC, solar cell, fuel cell and ultra-capacitor based cells are used as input sources and combination of dc sources are taken to generate multi-level output voltages.

In general, as compared with conventional inverter, the multi-level converter has the advantage i.e obtaining multi voltage levels with reduced switch count. As the voltage level number is increases to reach near shape of sinusoidal waveform with lower harmonic order. Different types of multi-level topologies available in literature like fly back, cascaded and diode clamped type converter. As these topologies required more switching count and produce higher harmonic level. In order to overcome these problems, this paper proposes new topology converter with reduced switches and generate 31 and 51 level voltages. A suitable sinusoidal and space vector modulated techniques implemented for generating gate signals for multi-level converter. These proposed systems are tested in MATLAB under different load conditions and compared the harmonic analysis.

II. Proposed Grid Connected PV System

Grid interfaced solar system with multi-level inverter is shown in Fig. 48.1.

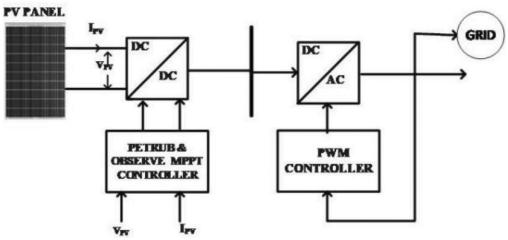

Fig. 48.1 Proposed Multi-Level Inverter with PV System

The architecture consists of the following components namely, (a) PV System, (b) MPPT based DC-DC Boost converter and (c) Modulation technique based multi-level converter for generating multi output voltage levels. In this Perturb and Observe MPPT technique is chosen.

A. Photovoltaic System

The PV system is a set of series and parallel connected solar cells to meet the requirement of panel. The output from the solar is not constant as it is depends on the climate conditions [8]. The main components in the proposed system are (a) DC-DC converter based PV system controlled by MPPT technique, (b) Wind Energy System with dc-dc converter, (c) PWM based Inverter.

The MPPT based DC-DC converter required for PV system as shown in Fig. 48.2. In this MPPT controller generates the reference signal based on the PV voltage and current [13]. This reference signal is compared with actual signal from the converter which is applied to PWM

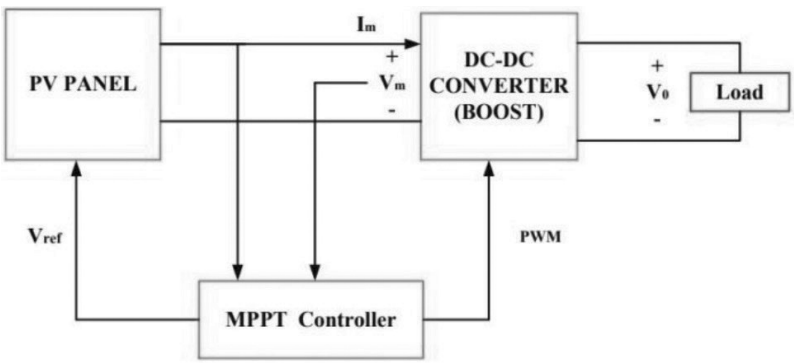

Fig. 48.2 Structure of MPPT based PV system

controller to generate suitable gate signal for dc-dc converter [14]. The power of a PV system is dependent on the local climate, thus in order to maximize solar PV output, the duty cycle must be adjusted such that it is applied to the gate pulse of the MOSFET/IGBT switch used in the boost converter.

The Photovoltaic current for solar cell is expressed as:

$$I = I_{ph} - I_o\left(e^{\frac{q(v+IR_s)}{NKT}} - 1\right) - \frac{(v+IR_s)}{R_{sh}} \qquad (1)$$

Figure 48.3, shows the closed loop controller for DC-DC boost converter of PV system. The Reference signal for modulation technique is generated using PV voltage and current parameters called as MPPT controller.

III. Proposed 31 Level Inverter

Figure 48.4 shows, the topology of multi-level inverter which generates 31-level output voltages. This configuration of 10 controlled switches with 4 levels of input dc voltage sources. The capacity of four sources are V_{A1} = V1, V_{B1} = 2*V1, V_{A2} = 5*V1 and V_{B2} = 10*V1. Out of 10 switches 8 switches form a bridge configuration with load for getting positive and negative of 15 level voltages and remaining Sp switch is turned for generating positive voltage, Sn is turn to generate negative voltages. In this way, there would be no spare switching combination performing in maximum number of voltage levels. Thus the relation between the values of the dc voltage sources used in the two corridor is as follows:

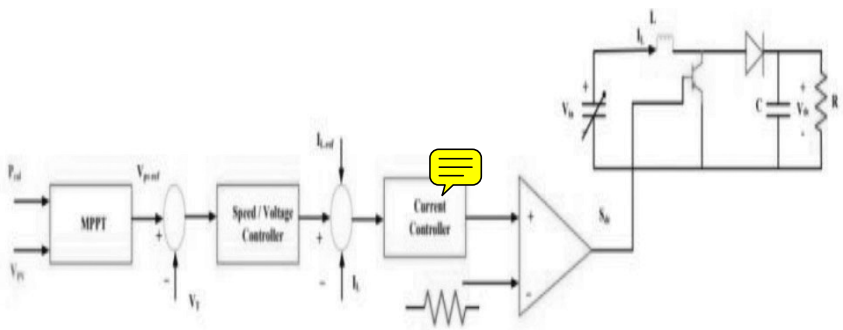

Fig. 48.3 MPPT based PWM controller for DC-DC converter

$$V_2 = \frac{n}{2}V_1 + V_1$$
$$= \left(\frac{n}{2}+1\right)V_1 \qquad (2)$$

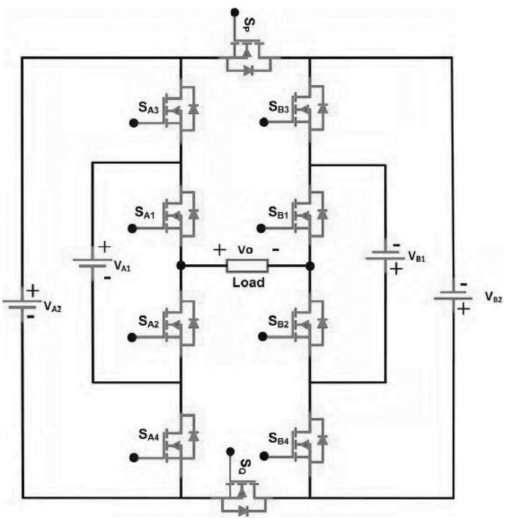

Fig. 48.4 Power Circuit of 31-level asymmetrical cascaded Inverter

The topology for 31-Level converter is shown in Fig. 48.4, it generates both positive and negative levels, the switch Sp helps to generate positive levels and the switch Sn helps to develop negative output voltage levels. The switching sequence for proposed 31-levels are indicated in Table 48.1. Different affair voltage situations can be generated according to this table. As the switches S1, S2, SP and the switches Sn1, Sn2, Sn are unidirectional, their diodes can conduct the current so that the current path is not disconnected anyway.

IV. Proposed Topology of 51 Level Inverter

In Fig. 48.5, shows the topology for 51-Level converter, which consists of reduced switches with 8 bi-directional switches and 4-unidirectional switches. The gate pattern required for 8 (Eight) switches are generated and made a comparison with two modulation techniques. The proposed 51-Level topology consists of 2 (Two) isolated dc sources V_a, V_b, with 8 power electronic switches S_{A1}, S_{A2}, S_{A3}, S_{A4}, S_{B1}, S_{B2}, S_{B3}, S_{B4}, and two diodes

Table 48.1 Switching State of 31-level Inverter

Voltage Level	Name and state of Switches				
	S_{A1}, S_{A2}	S_{A3}, S_{A4}	S_{B1}, S_{B2}	S_{B3}, S_{B4}	S_P, S_Q
0	1, 0	1, 0	1, 0	1, 0	0, 1
1	1, 0	1, 0	0, 1	1, 0	0, 1
2	0, 1	1, 0	1, 0	1, 0	0, 1
3	0, 1	1, 0	0, 1	1, 0	0, 1
4	1, 0	1, 0	1, 0	0, 1	0, 1
5	1, 0	1, 0	0, 1	0, 1	0, 1
6	0, 1	1, 0	1, 0	0, 1	0, 1
7	0, 1	1, 0	0, 1	0, 1	0, 1
8	1, 0	0, 1	0, 1	1, 0	0, 1
9	1, 0	0, 1	0, 1	1, 0	0, 1
10	0, 1	0, 1	1, 0	1, 0	0, 1
11	0, 1	0, 1	0, 1	1, 0	0, 1
12	1, 0	0, 1	1, 0	0, 1	0, 1
13	1, 0	0, 1	0, 1	0, 1	0, 1
14	0, 1	0, 1	1, 0	0, 1	0, 1
15	1, 0	1, 0	1, 0	1, 0	0, 1
-1	1, 0	1, 0	1, 0	1, 0	1, 0
-2	0, 1	1, 0	1, 0	1, 0	1, 0
-3	0, 1	1, 0	0, 1	1, 0	1, 0
-4	0, 1	1, 0	1, 0	0, 1	1, 0
-5	1, 0	0, 1	1, 0	1, 0	1, 0
-6	0, 1	0, 1	0, 1	0, 1	1, 0
-7	0, 1	1, 0	0, 1	0, 1	1, 0
-8	1, 0	0, 1	0, 1	1, 0	1, 0
-9	1, 0	0, 1	0, 1	1, 0	1, 0
-10	0, 1	0, 1	1, 0	1, 0	1, 0
-11	0, 1	0, 1	0, 1	1, 0	1, 0
-12	1, 0	0, 1	1, 0	0, 1	1, 0
-13	1, 0	0, 1	0, 1	0, 1	1, 0
-14	0, 1	0, 1	1, 0	0, 1	1, 0
-15	0, 1	0, 1	0, 1	0, 1	1, 0

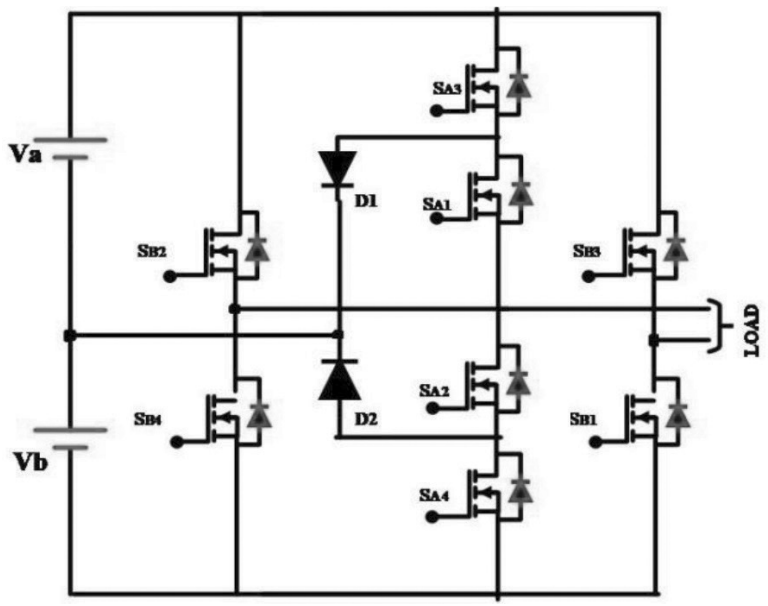

Fig. 48.5 Power circuit of proposed topology of 51-level asymmetrical cascaded Inverter

D_1, D_2. This asymmetrical multilevel Inverter topology produces 51 levels, i.e., 25 positive levels, 25 negative situations and a zero level. The positive terminal of the switch is connected between the switches S_{B2}, S_{B4} and negative switches connected between the switches S_{B1}, S_{B3}. Diode D_1 is conducted for positive cycle and D_2 conduct for negative part.

The equations for identifying the number of switches, gate driver circuits and number of voltage are shown below

$$N_{sw} = 2k + 4$$
$$N_{gd} = 3k + 4$$
$$N_l = 25k + 1 \quad (3)$$

The peak Output Voltage is given by

$$V_{o,m} = (12k + 1)V_{dc} \quad (4)$$

A. Space Vector Modulation Technique

Space vector modulation based technique is one of the type in pulse modulation techniques has the advantage of low harmonic content. In this technique the reference signal is divided in to eight vector components namely V0, V2, V3 and . . . V7. Here, V0 and V7 vectors called as null vectors and V1 to V6 vectors are decide the switching sequence of switches in converter.

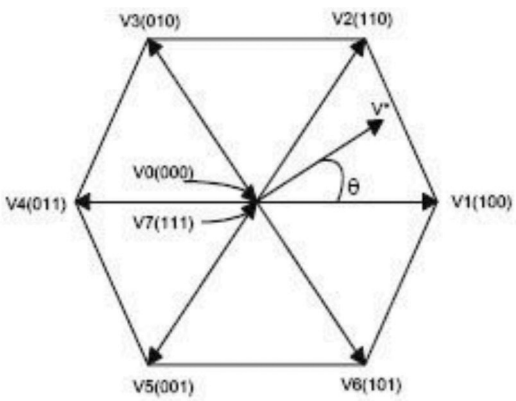

Fig. 48.6 Space Vector Modulation Technique

In Fig. 48.6, the vector V1 has coordinates of (1,0,0) which decides that Phase-a is in "ON" position while phase-b and phase-c are in "OFF" position. The required pulse width is identified by considering the position of particular reference signal between the two

vectors during a period of time. The expression for calculating pulse width is identified by the following time duration T_1, T_2 and T_0.

Table 48.2 Switching State of Proposed 51-level Inverter

Voltage Level	Name and state of Switches				
	S_{A1}, S_{A2}	S_{A3}, S_{A4}	S_{B1}, S_{B2}	S_{B3}, S_{B4}	D_1, D_2
0	1, 1	0, 0	0, 0	1, 0	1, 0
1	0, 1	1, 0	0, 0	1, 0	1, 0
2	1, 0	0, 1	0, 0	1, 0	1, 0
3	1, 0	0, 1	0, 0	1, 1	1, 0
4	0, 0	1, 0	1, 1	0, 0	1, 0
5	0, 1	0, 1	1, 0	1, 0	1, 0
6	1, 0	0, 1	0, 1	1, 0	1, 0
7	1, 0	1, 0	0, 1	1, 0	1, 0
8	0, 1	1, 0	1, 0	1, 0	1, 0
9	0, 1	0, 0	0, 0	0, 1	1, 0
10	0, 1	0, 0	1, 0	0, 1	1, 0
11	1, 0	1, 0	0, 1	0, 1	1, 0
12	1, 0	0, 1	0, 0	0, 1	1, 0
13	0, 1	0, 0	1, 0	1, 0	1, 0
14	0, 0	0, 1	0, 0	1, 0	1, 0
15	1, 0	1, 0	0, 1	0, 1	1, 0
16	0, 0	1, 0	1, 0	0, 0	1, 0
17	0, 1	0, 0	1, 1	0, 1	1, 0
18	1, 0	0, 1	0, 0	1, 0	1, 0
19	0, 1	0, 0	1, 0	1, 0	1, 0
20	0, 1	1, 0	1, 0	0, 1	1, 0
21	0, 0	0, 1	0, 1	1, 0	1, 0
22	0, 0	0, 1	1, 0	1, 0	1, 0
23	1, 0	1, 0	0, 1	0, 1	1, 0
24	0, 1	0, 0	0, 0	1, 1	1, 0
25	0, 0	0, 0	1, 0	1, 0	1, 0
-1	0, 0	0, 1	1, 0	0, 1	0, 1
-2	0, 0	1, 1	0, 1	0, 0	0, 1
-3	1, 0	0, 1	0, 1	0, 1	0, 1
-4	0, 0	1, 1	0, 0	0, 0	0, 1
-5	1, 0	0, 1	0, 0	0, 1	0, 1
-6	0, 1	0, 0	1, 0	0, 1	0, 1
-7	0, 1	1, 0	0, 0	0, 0	0, 1
-8	1, 1	0, 0	0, 0	1, 1	0, 1
-9	0, 0	0, 0	1, 1	1, 0	0, 1
-10	0, 0	1, 0	0,1	1, 0	0, 1
-11	1, 0	0, 0	0, 1	1, 0	0, 1
-12	0, 0	0, 1	1, 0	1, 0	0, 1
-13	0, 0	1, 1	0, 0	1, 0	0, 1
-14	1, 0	0, 1	0, 0	1, 0	0, 1
-15	0, 1	0, 0	1, 0	1, 0	0, 1
-16	0, 1	1, 0	0, 1	0, 1	0, 1
-17	1, 1	0, 0	0, 1	0, 1	0, 1
-18	1, 0	0, 0	1, 0	0, 1	0, 1
-19	0, 1	0, 0	0, 1	0, 1	0, 1
-20	0, 0	0, 1	1, 0	0, 1	0, 1
-21	0, 0	1, 1	0, 0	0, 1	0, 1
-22	1, 0	0, 1	0, 0	0, 1	0, 1
-23	0, 1	0, 0	1, 0	0, 1	0, 1
-24	0, 1	1, 0	0, 0	0, 1	0, 1
-25	1, 1	0, 0	0, 0	0, 1	0, 1

The reference signals for voltages and V_0 to V_7 and switch-ing time sequences are generated by the following expression:

$$V * T_z = (V_1 * T_1) + (V_2 * T_2) + \left(V_o * \left(\frac{T_0}{2}\right)\right) + \left(V_7 * \left(\frac{T_o}{2}\right)\right) \quad (5)$$

The expressions for calculations of switching and conduction losses for both IGBT and diode are shown below:

$$P_s = [V_s + R_s\, i^{\beta}(t)]i(t) \quad (6)$$

$$P_D = [V_D + R_D\, i^{\beta}(t)]i(t) \quad (7)$$

$$P_{sw,s} = [E_{on} + E_{off}]f_{sw} \quad (8)$$

$$P_{sw,D} = [E_{on,D} + E_{off,Df}]f_{sw} \quad (9)$$

V. Simulation Model

To verify and test the 31-Level based multi-level converter, this system is implemented in simulation. The values taken as R = 10 ohm and L = 25 mH.

The simulation result for 31-Level output voltage and current is shown in Fig. 48.7 under RL-Load, and the harmonic analysis is for voltage and current is shown in Fig. 48.8 and Fig. 48.9. The simulation diagram for space vector modulated based 51-Level based converter is implemented by diagram shown in Fig. 48.5. The switching Table 48.2 shows the different strategies of switching conditions to generate 51 level voltages. The output voltage of 51-Level converter is shown in Fig. 48.10 and the FFT harmonic analysis for load voltage and current with RL load is shown in Fig. 48.11 and Fig. 48.12.

VI. Conclusion

The design of multilayer inverters with fewer circuit components, minimal losses, cheap cost, and compact size with high efficiency had undergone a great deal more research. The type of multilevel inverter utilized in

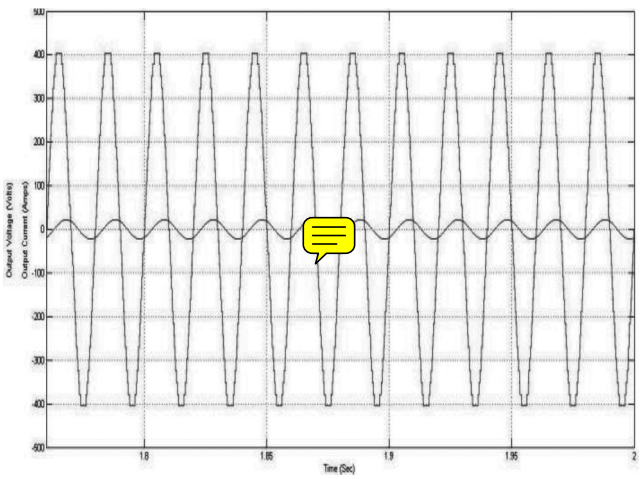

Fig. 48.7 Output Voltage and Current Waveforms of the 31 Level MLI for R_L load

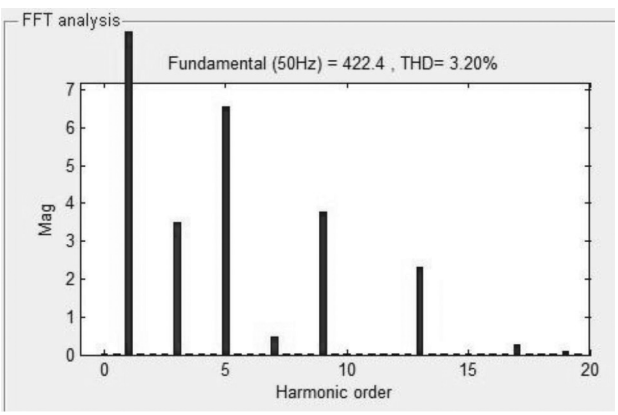

Fig. 48.8 FFT Analysis for Load Voltage with R_L Load of 31-level Inverter

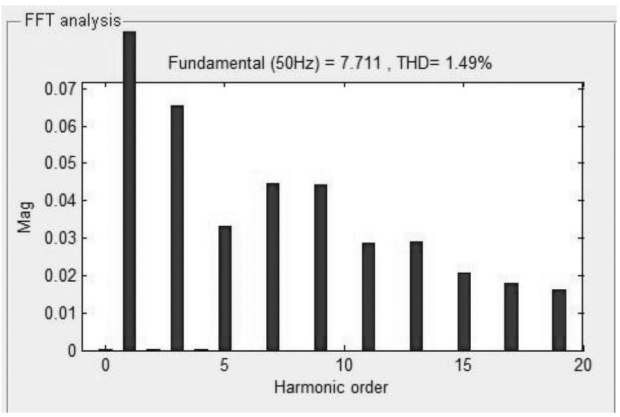

Fig. 48.9 FFT Analysis for Load Current with R_L Load of 31-level Inverter

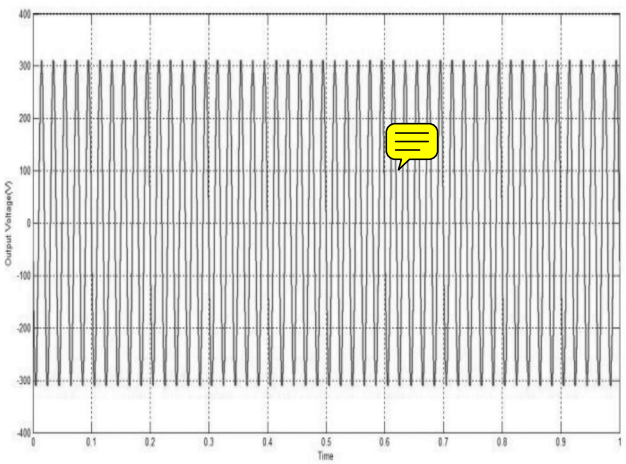

Fig. 48.10 Output Voltage and Current Waveforms of the 51 Level MLI for R_L load

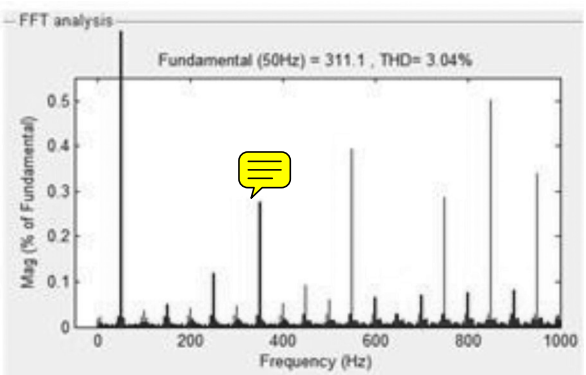

Fig. 48.11 FFT Analysis for Load Voltage with R_L load of 51-level Inverter

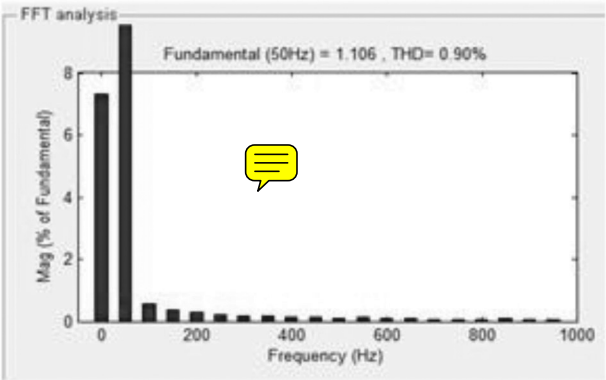

Fig. 48.12 FFT Analysis for Load Current with R_L load of 51-level Inverter

high and medium power applications, such as electric vehicles, power drives, grid integration systems, etc., is surveyed in this study. To identify the difficulties and important problems, a thorough analysis of the most recent multilevel inverter design with fewer switches is undertaken. The amount of diodes, switches, source utilization, and filter requirements are mentioned as significant difficulties of various multilevel inverter systems. This paper shows a novel configuration of MLIs. The proposed MLI system consists of lower number of switches than given conventional inverter circuit configuration, and has no additional equipment such as inductors and capacitors. A new 31-level and 51-level switched inverter is configured using MATLAB/Simulink. To test the robustness of the proposed scheme, a load disturbances test is conducted. It is observed that the proposed 51-level topology is well stabilized under load disturbances conditions.

VII. Acknowledgment

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Power Quality Improvement in Microgrid System Using PSO-Based UPQC Controller

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Abstract

This chapter proposes a concept of new control techniques for unified power quality conditioner to improve the power quality in microgrid system. Here, wind energy system is considered for designing of microgrid system. In this chapter a SCIG based wind energy system is considered as one of the DG source. To get maximum reliability from wind energy system an MPPT based DC–DC converter is implemented. For improving power quality of the proposed microgrid system, this chapter is implemented with unified power quality conditioner. Suitable control techniques are designed for both series and shunt converters of UPQC. To achieve better power quality improvement under different load conditions a PSO optimization technique is implemented in this chapter. This proposed microgrid system with UPQC controller under different controllers are implemented and tested in MATLAB.

Keywords: Grid-connected system, optimization technique, power quality, custom power device, MPPT and wind energy system

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